Di Wu

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1415 Engineering Dr, Madison, WI 53706, USA

Education

Doctor of Philosophy | ***Electrical and Computer Engineering*** Sep. 2017 – May 2023 (Expected)
University of Wisconsin–Madison Madison, WI, USA

- Advisor: Joshua San Miguel
- Thesis: Unary Computing for Power-Efficient Computer Architecture

Master of Engineering | ***Microelectronics*** Sep. 2012 – Jan. 2015
Fudan University Shanghai, China

Bachelor of Science | ***Microelectronics*** Sep. 2007 – Jul. 2012
Fudan University Shanghai, China

Research Interest

- Emerging computer architecture
- Deep neural network acceleration
- Brain computer interface
- Fault-tolerant quantum computing
- Unary computing
- Neuromorphic computing
- Approximate computing
- Reconfigurable computing

Honors and Awards

Capstone PhD Teaching Award Nomination 2022
UW–Madison

Grainger Wisconsin Distinguished Graduate Fellowship (1 out of 3) 2022
College of Engineering, UW–Madison

Student Travel Award 2022
International Symposium on Computer Architecture (ISCA)

Dissertator Travel Award (twice) 2022
Department of Electrical and Computer Engineering, UW–Madison

Ph.D. Forum at Design Automation Conference (DAC) 2021
Special Interest Group on Design Automation (SIGDA)

IEEE Micro Top Pick (1 out of 12) 2021
Selected from all Computer Architecture Publications in 2020

Gerald Holdridge Outstanding Teaching Assistant Award 2020
Department of Electrical and Computer Engineering, UW–Madison

Chancellor's Opportunity Fellowship 2019
UW–Madison

Student Research Travel Award 2019
UW–Madison

Student Research Competition Travel Award 2019
International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)

Student Travel Award 2019
International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)

Qualcomm Innovation Fellowship Finalist 2019
Qualcomm

Foxconn SmartCity Competition Winner 2019
Foxconn

Hiran Mayukh Award 2018
UW–Madison Computer Architecture Community

Rising Star Award 2015
HiSilicon

National Scholarship (ranking 1/67) 2015
Fudan University

Excellent Student Union Leader (as Sports Minister) 2010
Zhangjiang Campus, Fudan University

Third Prize Freshman Scholarship (ranking 3/45) 2007
Fudan University

PUBLICATIONS

Conference

[1] uBrain: A Unary Brain Computer Interface [Acceptance rate=16.8%]
Di Wu, Jingjie Li, Zhewen Pan, Younghyun Kim, Joshua San Miguel
International Symposium on Computer Architecture (ISCA), 2022

[2] uSystolic: Byte-Crawling Unary Systolic Array [Acceptance rate=30.5%]
Di Wu, Joshua San Miguel
International Symposium on High-Performance Computer Architecture (HPCA), 2022
Open-source software: uSystolic-Sim

[3] When Dataflows Converge: Reconfigurable and Approximate Computing for Emerging Neural Networks [Invited]
Di Wu, Joshua San Miguel
International Conference on Computer Design (ICCD), 2021

[4] UNO: Virtualizing and Unifying Nonlinear Operations for Emerging Neural Networks [Acceptance rate=26.4%]
Di Wu, Jingjie Li, Setareh Behrooz, Younghyun Kim, Joshua San Miguel
International Symposium on Low Power Electronics and Design (ISLPED), 2021

[5] Normalized Stability: A Cross-Level Design Metric for Early Termination in Stochastic Computing [Acceptance rate=30.2%]
Di Wu, Ruokai Yin, Joshua San Miguel
Asia and South Pacific Design Automation Conference (ASP-DAC), 2021

[6] uGEMM: Unary Computing Architecture for GEMM Applications [Acceptance rate=18.3%]
Di Wu, Jingjie Li, Ruokai Yin, Hsuan Hsiao, Younghyun Kim, Joshua San Miguel
International Symposium on Computer Architecture (ISCA), 2020
Open-source software: UnarySim
Awarded 1 out of 12 IEEE Micro Top Picks 2021 from all computer architecture publications in 2020

[7] Approximate Hardware Techniques for Energy-Quality Scaling Across the System [Invited]
Younghyun Kim, Joshua San Miguel, Setareh Behroozi, Tianen Chen, Kyuin Lee, Yongwoo Lee, Jingjie Li, **Di Wu**
International Conference on Electronics, Information, and Communication (ICEIC), 2020

[8] SECO: A Scalable Accuracy Approximate Exponential Function Via Cross-Layer Optimization [Acceptance rate=35.2%]
Di Wu, Tianen Chen, Chienfu Chen, Oghenefego Ahia, Joshua San Miguel, Mikko Lipasti, Younghyun Kim
International Symposium on Low Power Electronics and Design (ISLPED), 2019

[9] In-Stream Stochastic Division and Square Root via Correlation [Acceptance rate=18.9%]
Di Wu, Joshua San Miguel
Design Automation Conference (DAC), 2019

[10] Convergence-Optimized Variable Node Structure for Stochastic LDPC Decoder
Qichen Zhang, Yun Chen, **Di Wu**, Xiaoyang Zeng, Yeong-luh Ueng
International Conference on Acoustics, Speech and Signal Processing (ICASSP), 2016

[11] An Area-Efficient Architecture for Stochastic LDPC Decoder
Qichen Zhang, Yun Chen, **Di Wu**, Xiaoyang Zeng, Yeong-luh Ueng
International Conference on Digital Signal Processing (DSP), 2015

[12] Latency-Optimized Stochastic LDPC Decoder for High-Throughput Applications
Di Wu, Yun Chen, Qichen Zhang, Lirong Zheng, Xiaoyang Zeng, Yeong-luh Ueng
International Symposium on Circuits and Systems (ISCAS), 2015

[13] A High-Throughput LDPC Decoder for Optical Communication
Di Wu, Yun Chen, Yuebin Huang, Yeongluh Ueng, Lirong Zheng, Xiaoyang Zeng
International Conference on ASIC (ASICON), 2013

Journal

[1] uGEMM: Unary Computing for GEMM Applications [Acceptance rate=9.9%]
Di Wu, Jingjie Li, Ruokai Yin, Hsuan Hsiao, Younghyun Kim, Joshua San Miguel
IEEE Micro 41.3 (2021), pp. 50–56
IEEE Micro Top Pick Issue 2021

[2] In-Stream Correlation-Based Division and Bit-Inserting Square Root in Stochastic Computing
Di Wu, Ruokai Yin, Joshua San Miguel
IEEE Design & Test 38.6 (2021), pp. 53–59

[3] Strategies for Reducing Decoding Cycles in Stochastic LDPC Decoders
Di Wu, Yun Chen, Qichen Zhang, Yeong-luh Ueng, Xiaoyang Zeng
IEEE Transactions on Circuits and Systems II: Express Briefs 63.9 (2016), pp. 873–877

[4] An Efficient Multirate LDPC-CC Decoder With a Layered Decoding Algorithm for the IEEE 1901 Standard
Yun Chen, Qichen Zhang, **Di Wu**, Changsheng Zhou, Xiaoyang Zeng
IEEE Transactions on Circuits and Systems II: Express Briefs 61.12 (2014), pp. 992–996

Workshop

[1] T-MAC: Temporal Multiplication with Accumulation
Zhewen Pan, **Di Wu**, Joshua San Miguel
Young Architect Workshop (YArch), collocated with International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS) (2022)

Pre-Print

[1] Representation Range Needs for 16-Bit Neural Network Training
Valentina Popescu, Abhinav Venigalla, **Di Wu**, Robert Schreiber
arXiv Pre-print (2021)

Open-Source Software

GitHub

[1] uSystolic-Sim: A Simulator for Weight Stationary Systolic Arrays with Multiple MAC Cycles and Varying Bitwidth
"uSystolic: Byte-Crawling Unary Systolic Array", *HPCA* 2022

[2] UnarySim: A Simulator for General Unary Computing
"uGEMM: Unary Computing Architecture for GEMM Applications", *ISCA* 2020

Invited Talks

Power-Efficient Computer Architecture via Unary Computing — Oct. 2022
University of California, Santa Barbara (Virtual) — Santa Barbara, CA, USA

uBrain: A Unary Brain Computer Interface — Nov. 2022
University of Central Florida (Virtual) — Orlando, FL, USA

Power-Efficient Computer Architecture via Unary Computing — Nov. 2022
University of California, Los Angeles (Virtual) — Los Angeles, CA, USA

Employment

Research Assistant — Sep. 2017 – Now
Department of Electrical and Computer Engineering, UW–Madison — Madison, WI, USA

- Unary computing
  - Universal general matrix multiply (GEMM) operations
  - Metric-guided design methodology
  - Open-source simulators
  - Unary deep learning architecture
  - Algorithm-hardware co-design methodology
  - Unary brain computer interface architecture
- Approximate and reconfigurable computing
  - Reconfigurable nonlinear approximation
  - Systolic array with hybrid dataflows for GEMM and nonlinear operations

Research Intern — May 2022 – Sep. 2022
Cerebras Systems — Sunnyvale, CA, USA

- Wafer-scale computer architecture for deep learning
  - Wafer-scale power-performance projection
  - Nonlinear operation vectorization

Research Intern May 2020 – Sep. 2020
Cerebras Systems Sunnyvale, CA, USA

- Novel 16-bit FP (CB16) format for deep learning training

Research Intern May 2019 – Sep. 2019
Meta (Formerly Facebook) Sunnyvale, CA, USA

- Deep learning quantization
  - Post-training quantization
  - Quantization-aware training

Digital Circuit Engineer Mar. 2015 – May 2017
HiSilicon Shanghai, China

Research Assistant Sep. 2012 – Jan. 2015
State Key Laboratory of ASIC and System, Fudan University Shanghai, China

- Low-density Parity-Check (LDPC) decoder architecture

Teaching and Mentoring

Teaching Assistant

ECE554 (Digital Engineering Lab), UW–Madison	Spring 2022, Spring 2020, Fall 2019, Spring 2019, Fall 2018
ECE454 (Mobile Computing Lab), UW–Madison	Fall 2021, Fall 2020
ECE552 (Introduction to Computer Architecture), UW–Madison	Fall 2018

Guest Lecturer

ECE757 (Advanced Computer Architecture II), UW–Madison	Spring 2021, Spring 2020
ECE752 (Advanced Computer Architecture I), UW–Madison	Spring 2019

Student Mentor

(Graduate) Unary computing: Deep learning architecture, UW–Madison	2022 – Now
(Undergraduate) Unary computing: Brain computer interface architecture, UW–Madison	2021 – Now
(Undergraduate) Unary computing: Metric-guided design methodology, UW–Madison	2019 – 2021

Professional Service

Committee Member

Young Architect Workshop (YArch)	2023
International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS) – Artifact Evaluation	2021, 2020
International Symposium on Microarchitecture (MICRO) – Artifact Evaluation	2021

Conference Reviewer

International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS)	2023

International Symposium on Computer Architecture (ISCA) 2023, 2022, 2020, 2019

International Symposium on High-Performance Computer Architecture (HPCA) 2021

International Symposium on Microarchitecture (MICRO) 2022, 2021, 2019

Design Automation Conference (DAC) 2020, 2018

International Symposium on Circuits and Systems (ISCAS) 2023, 2022

Program Mentor

International Symposium on Microarchitecture (MICRO) – "Meet a Senior PhD Student" 2020

Professional Development

NSF Funding: Why, What and How with Computer Sciences Professor Oct. 2022
School of Computer, Data & Information Sciences, UW–Madison Madison, WI, USA

Diversity, Equity and Inclusion

Student Volunteer 2010
Expo 2010 Shanghai China Shanghai, China

Sports Minister 2009
Zhangjiang Campus, Fudan University Shanghai, China

Volunteer Caregiver 2008
Shanghai Guanxin School (for students with disabilities) Shanghai, China